An Improved Interleaved Boost Converter With PSO-Based Optimal Type-III Controller

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***Abstract*— This paper presents an improved interleaved boost converter (IBC) with optimal Type-III controller by utilizing voltage mode control. Due to the presence of several power switches in parallel path, the degree of freedom has been increased in IBC. Also, the IBC produces lower output voltage ripples, so the size and losses of the output filter can significantly be reduced compared with conventional BC. But due to the *nonminimum phase* problem of IBC, closed-loop bandwidth is restricted that causes slower converter dynamics. It is difficult for the conventional proportional–integral–differential controller to exhibit good performance with line, load changes, and parametric uncertainty. So an optimal Type-III controller is designed and implemented for achieving better closed-loop dynamic performance and stability. Initially, controller parameters have been designed by using the classical "*k-factor*" method, and then particle swarm optimization-based optimal Type-III controller is developed for the proposed IBC. The comparative closed-loop performances of BC and IBC with classical and optimal Type-III controllers have been presented. The proposed control scheme by utilizing the optimized Type-III controller in IBC is newly introduced in this paper and has not been reported earlier. The overall control circuit diagram using voltage-mode controlled two-phase IBC has been implemented by simple analog control circuit and the cost of complete experimental setup is very cheap. Simulation and experimental results have been produced to show the efficacy of the proposed converter control system.**

***Index Terms*— Interleaved boost converter (IBC), nonminimum phase system, optimal type-III controller, particle swarm optimization (PSO), switched-mode-power-supply (SMPS).**

I. Introduction

THE interleaved boost converter (IBC) is made by connecting several identical BCs in parallel [1], [2]. The switch of each BC is controlled by the interleaved gate pulse. The frequencies of the gate pulses are similar to the switching frequency but the phases of the control signals are shifted according to the firing logic. In IBC, the input current is shared among the parallely connected switches so the reliability and efficiency of the converter is relatively higher compared with normal BC. Due to the presence of several power switches in parallel path, the degree of freedom has been increased in IBC that implies the improvement of some important aspects, such as repairing and maintenance, loss-heat dissipation, and fault tolerance [3]. Also, the IBC produces lower output voltage ripples, so the size and losses of the output filter can significantly be reduced compared with normal BC. In interleaving technique, the control signals are generally phase sifted each other with similar switching frequency. So, the resultant input and output current waveforms contain lower ripple with smaller harmonics content than normal BC. Due to the cancellation of low-frequency harmonics, the conduction and switching losses and electromagnetic interference levels decrease significantly in IBC.

In a two-phase converter, there are two output stages that are driven 180° out of phase. By splitting the current into two power paths, conduction losses can be reduced, increasing overall efficiency compared with a single-phase converter. Because the two phases are combined at the output capacitor, effective ripple frequency is doubled, making ripple voltage reduction much easier. Likewise, power pulses drawn from the input capacitor are staggered, reducing ripple current requirements.

In the field of power electronics, the application of interleaving technique can be traced back to very early days, especially in high-power applications. In high-power applications, the voltage and current stress can easily go beyond the range that one power device can handle. Multiple power devices connected in parallel and/or series could be one solution. However, voltage sharing and/or current sharing are still the concerns. Instead of paralleling power devices, paralleling power converters is another solution which could be more beneficial. Furthermore, with the power converter paralleling architecture, the interleaving technique comes naturally. Benefits such as harmonic cancellation, better efficiency, better thermal performance, and high power density can be obtained [4].

For high-power applications, in order to meet certain system requirement, interleaving multichannel converter could be a superior solution especially considering the available power devices with limited performance. One of such example can be found in the application of superconducting a magnetic energy storage system (MES) [5]. The current stress of such application is extremely high, yet certain system performance still need to be met. On the ac side, the total harmonic distortion in voltages and currents of the regulatory standards must be respected. Such examples can also be found in many other applications, design of switched-mode-power-supplies (SMPSs), automobile engineering, power modules of spacecraft, satellite or avionic applications, hybrid electrical vehicles, static VAR generator (SVG), High Voltage

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Direct Current (HVDC) applications, and so on [6]–[8]. For maximum power extraction from solar photovoltaic (SPV) panels, the usage of IBC may be beneficial due to its fast transient response and absence of high frequency ripple that may interact with the SPV system [9]. They are used in applications where the loads demand low ripple or very tight tolerances. Such requirements are found in new generation of personal computers, in which core voltages and currents of the central processing units are approaching 1 V and 130 A, respectively. Interleaving converters are also finding applications in switching audio amplifiers by interleaving series or parallel combinations of power inverters [10].

A number of research works based on two-phase IBC have been done and reported in the literature [11]–[36]. When the number of phase in IBC is more, the circuit design will be more complicated. So, two-phase IBC in continuous conduction mode (CCM) is considered in this paper for simplicity.

Over the past few years, the dc–dc switching converter technology has undergone tremendous changes. Very fast transient response is needed for switched mode power converters to feed new generation microprocessors and DSPs, electrical vehicles, integration of different renewable energy sources in grid, and so on. So, the transient performance is an important issue in closed-loop converter for designing the practical power supplies. But some converters (such as BC, IBC, and so on) have a right-half-plane (RHP) zero, present in their control-to-output transfer function for the CCM of operation. So, an initial undershoot has been observed for a step input in these converters and those converters suffer from poor dynamic performance due to the presence of *nonminimum phase* problem [37]. These undesirable undershoot becomes more prominent if the RHP zero moves closer to the origin. This RHP zero limits the closed-loop bandwidth that causes slower converter dynamics.

But conventional proportional–integral–differential (PID) controllers cannot solve this nonminimum phase problem completely. In this paper, classical Type-III controller is designed for IBC by using "*k-factor*" approach [38]–[40] and this paper has been extended to BC. Then, the tuning of controller parameters has been performed by using the *particle swarm optimization* (PSO) [41]–[44] technique for obtaining better closed-loop performance and stability for converters.

The algorithms for designing optimal controllers are normally inspired by several physical mechanism, such as behavior and characteristics of biological, molecular, swarm of insects, neurobiological systems, and so on [39]. There is no specific algorithm to achieve the best solution for all optimization problems. Some algorithms may give better solution for some specific problems than others. In this paper, the PSO technique is used to design the optimized Type-III controller for two-phase IBC. This algorithm of PSO is population-based optimization techniques and simple to realize and easily implementable. Some of the optimized methods [45]–[55] have been applied for the controllers deign of converters, but PSO-based optimal Type-III controller for IBC is newly introduced in this paper. In this paper, the closed-loop BC and IBC with optimal Type-III controller have been designed and fabricated in laboratory. The simulated and experimental results have been presented to show the effectiveness of the optimized controller for the proposed converters.

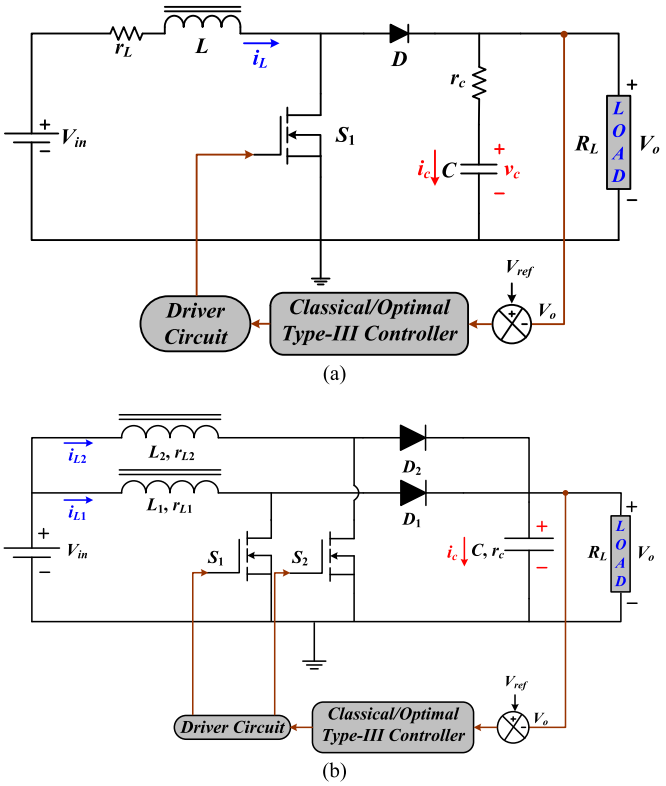


Fig. 1. Schematic of (a) closed-loop conventional BC and (b) closed-loop two-phase IBC.

II. Description and Modeling of Boost and Two-Phase Interleaved Boost Converters

In this section, the modeling of conventional BC and IBC is discussed. Modeling of converters is very much required for the controller design. The block diagram representations of the voltage mode control of BC and two-phase IBC are shown in Fig. 1(a) and (b), respectively. In BC (Fig. 2), two modes of operation have been observed in CCM. But in the case of IBC, there are two controlled switches, S_1 and S_2. So, there are four modes of operation (Fig. 3): Mode-I, Mode-II, Mode-III, and Mode-IV. From Fig. 1, it can be observed that the output voltage of the converter is sensed and compared with reference voltage; an error signal is generated and is passed through the proposed classical/optimized Type-III controller which generates the control signal. Then, the control signal is compared with the high-frequency triangular waveform to produce Pulse Width Modulation (PWM) signal. This PWM signal is passed through a driver circuit and the signal drives MOSFET switches (S_1, or S_1 and S_2) after passing through the optoisolator and astable-multivibrator circuits. Since both the converters are embedded in the same printed circuit board (PCB), for the testing of BC, the gate pulse of the MOSFET, S_2 will be turned OFF.

The switching power converters are inherently time varying and highly nonlinear in nature. State-space averaging (SSA) method is a well-known procedure that is used to approximate

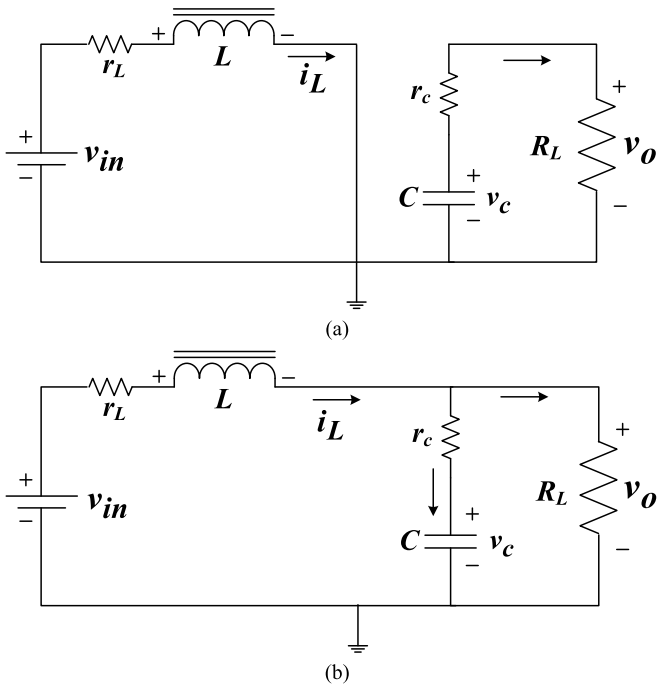


Fig. 2. Equivalent circuit of a BC. (a) Mode-I. (b) Mode-II.

the converters derivation in continuous linear domain. In SSA techniques, the corner frequency (f_{corner}) of the output filter to be much smaller than the converter's switching frequency (f_{sw}) (i.e., $f_{\text{corner}}/f_{\text{sw}} \ll 1$) [39]. From the SSA technique, the mathematical modeling can be found from the equivalent circuit model of the converter. The small-signal transfer functions can be derived from the mathematical model of the switching converter. The major advantages of this method are the establishment of a complete converter model with both steady-state and dynamic quantities [39]. The goal of the following analysis is to obtain a small signal transfer function $\tilde{v}_o(s)/\tilde{d}(s)$, where $\tilde{v}_o$ and $\tilde{d}$ are small perturbations in the output voltage v_o and duty ratio d of the converter.

A. State Space Averaging Model of Boost Converter

In BC, there are two operating intervals, i.e., *boost* interval, dT_{sw}, and *capacitor charging* interval, $d'T_{\text{sw}}$ in CCM, where T_{sw} is switching period; d and d' are duty ratio at boost and capacitor charging interval, respectively. So $d + d' = 1$. The sequence of the intervals of operation can be defined as $d \rightarrow d'$. The equivalent circuit of a BC is shown in Fig. 2. In the equivalent circuit, the elements are defined as follows: v_{in}, v_o, L, C, r_l, r_c, and R_L are input voltage, output voltage, inductance, output capacitance, inductor resistance, Equivalent Series Resistance (ESR) of capacitor, and load resistance, respectively.

The control-to-output transfer function of BC can be derived by using the SSA model [39] and the desired transfer function $T_{p\_\text{Boost}}(s)$ is given in the following:

$$T_{p\_\text{Boost}}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{V_{\text{in}}}{(1-D)^2} \times \frac{(1+sr_cC)\left(1 - s\frac{L}{(1-D)^2(R_L - r_L)}\right)}{\left[1 + s\frac{R_L\{r_LC(R_L+r_c)+L\}}{(R_L+r_c)[r_L+(1-D)^2R_L]} + \frac{s^2LCR_L}{r_L+(1-D)^2R_L}\right]}. \quad (1)$$

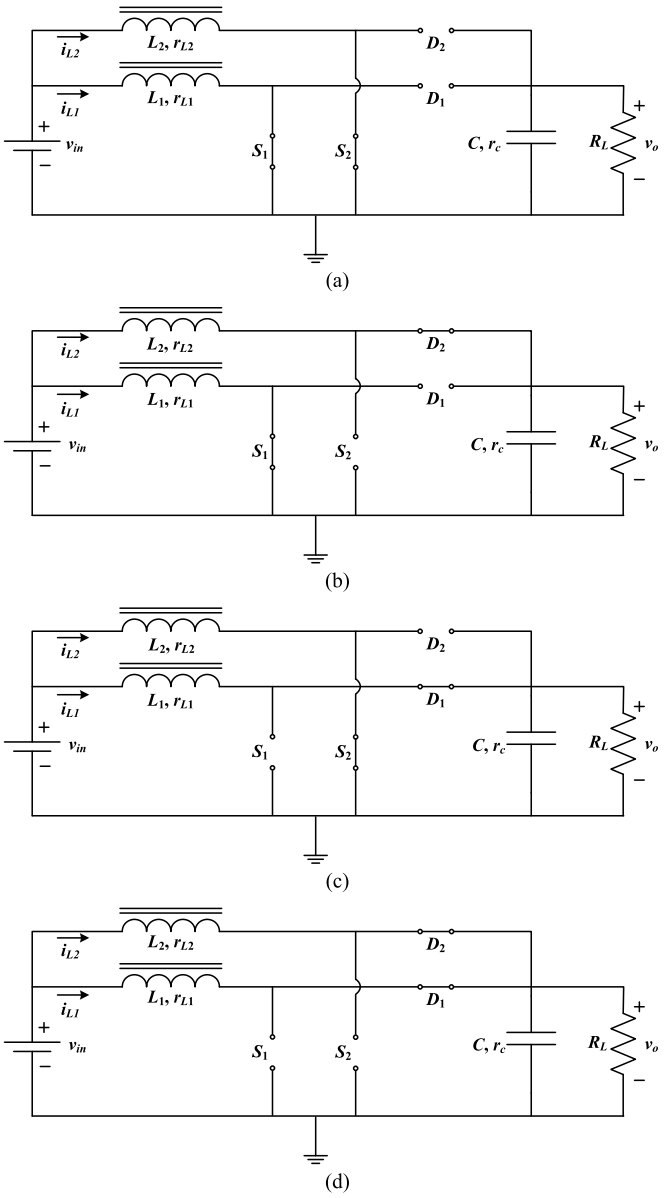


Fig. 3. Equivalent circuit of a two-phase IBC. (a) Mode-I, (b) Mode-II, (c) Mode-III, and (d) Mode-IV operations.

From (1), it can be noticed that an RHP *zero* exists in the transfer function of the BC plant.

B. State Space Averaging Model of Two-Phase Interleaved Boost Converter

Two-phase IBC having four modes of operations: Mode-I, d_1T_{sw}, Mode-II, d_2T_{sw}, Mode-III, d_3T_{sw}, and Mode-IV, d_4T_{sw}, where d_1, d_2, d_3, and d_4 are duty ratios at different intervals. It may be noted that $d_1+d_2+d_3+d_4 = 1$. The sequence of the intervals of operation can be defined as $d_1 \rightarrow d_2 \rightarrow d_3 \rightarrow d_4$. In this paper, it has been considered that $d_1 + d_2 + d_3 = d$ and $d_3 = d'$. The equivalent circuit of a two-phase IBC is shown in Fig. 3. In the equivalent circuit, the elements are defined as follows: v_{in}, v_o, L_1, L_2, C, r_{L1}, r_{L2}, r_c, and R_L are input voltage, output voltage, inductances, output capacitance, inductor resistances, ESR of capacitor, and load resistance, respectively.

TABLE I
PARAMETERS OF CONVERTERS

Circuit Components	Values
Input Voltage, V_{in}	5 Volt
Output Voltage, V_o	12 Volt
Reference Voltage, V_{ref}	12 Volt
Inductors, L_1 and L_2	275 μH
Output Filter Capacitor, C	470 μF
Inductor Resistance, r_{L1}, r_{L2}	0.4 Ω
ESR of Capacitor, r_c	0.4 Ω
Load Resistance, R_L	25 Ω
Switching frequency, f_{sw}	20 kHz

Using the SSA technique [3], control-to-output transfer function of IBC (T_{p_IBC}) can be obtained and the final form is given in the following:

$$T_{p\_\mathrm{IBC}}(s) = \frac{\tilde{v}_o(s)}{\tilde{d}(s)} = \frac{2NV_{\mathrm{in}}}{(r+2Nd'^2R_L)C} \times \frac{-s+(2Nd'^2R_L-r)/L_c}{\left(s+\frac{r}{L_c}\right)\left(s+\frac{1}{R_LC}\right)+\frac{2Nd'^2}{L_cC}} \quad (2)$$

where d = duty ratio, $d' = (1-d)$, $L_1 = L_2 = L_c$, $r_{L1} = r_{L2} = r$, and N = number of phase in interleaved converter.

It is clear that one RHP zero is present in the transfer function of the IBC of (2).

After putting the parameters of converters from Table I, the transfer functions of BC and IBC are found and these are given in the following:

$$T_{p\_\mathrm{Boost}}(s) = \frac{-0.19974(s-2.255\times10^4)(s+9259)}{(s^2+800.8s+1.737\times10^6)} \quad (3)$$

$$T_{p\_\mathrm{IBC}}(s) = \frac{-0.0023893(s-6.269\times10^4)}{(s^2+3.135s+5.53)}. \quad (4)$$

III. CONTROLLER DESIGN

The controller is necessary to achieve the desired closed-loop performances of the converter. The controller can also serve to shape the loop transfer function to achieve a necessary transient response and overall system stability. There are several typical types of analog compensation consisting of an amplifier and *RC* network. Lead compensator is also called proportional–derivative (PD) controller, which is usually utilized to improve the phase margin in a system originally consisting of a two poles. The possible side effect of PD controller is that it is sensitive to noise due to the derivative function.

Lag compensator [also called proportional–integral (PI)] is used to increase the low frequency loop gain, such that the output is better regulated at dc and at frequencies well below the loop crossover frequency. Combined PID controller is to obtain both wide bandwidth and large dc loop gain for reduced steady-state error.

There are several classical controllers, such as PI, PID, lead–lag, and so on, which have been developed over the years to ensure the desired performance of the converter under specific conditions. But in the case of IBC, an RHP zero is present in control-to-output transfer function for the CCM of operation. So, the IBC converters suffer from poor dynamic performance due to the presence of nonminimum phase problem. This RHP zero limits the closed-loop bandwidth that causes slower converter dynamics. So, it is difficult for the conventional PID controller to exhibit good performance with line, load changes, and parametric uncertainty. Type-controllers [38]–[40] are reported to improve the dynamic performances for these classes of dc–dc converters.

A. Design of Classical Type-III Controller

The "Type-III" controller is a lead–lead controller with a pole at origin. The pole at the origin provides a very high gain at low frequencies and the pole–zero pairs reduce the phase shift between the frequency of the two zeros and the frequency of two poles as lead controller. So, this controller provides 0° to 180° phase boost with zero steady-state error. Even though IBC having nonminimum phase problem, it exhibits a better closed-loop performance by utilizing a cascaded Type-III controller. With proper tuning of the controller parameters, the fastest closed-loop performance can be achieved with minimal overshoots and zero steady-state error [38]. The basic structure of a Type-III controller is shown in Fig. 4(a). The Type-III controller is intended for switching converters that exhibit a −40 dB/decade roll-off above the poles of the output filter and a −180° phase lag. Type-III controller network introduces zeros into the error amplifier to reduce the steep gain slope above the double pole caused by the filter and its associated 180° phase shift. This extends the loop bandwidth. Type-III controller network can achieve a very fast dynamic response.

B. Mathematical Approach

From the circuit diagram (Fig. 4), the transfer function of the Type-III controller can be written as

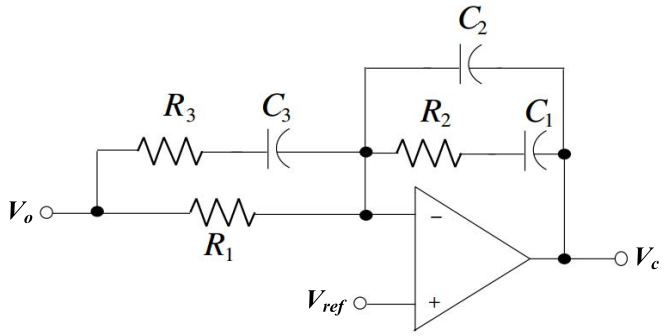
$$T_{c\_T\text{-III}}(s) = \frac{(1+s/\omega_{z1\_T\text{-III}})(1+s/\omega_{z2\_T\text{-III}})}{(s/\omega_{p0\_T\text{-III}})(1+s/\omega_{p1\_T\text{-III}})(1+s/\omega_{p2\_T\text{-III}})}. \quad (5)$$

The controller having one pole (f_{p0_III}) at zero and other two high-frequency poles, one at $f_{p1\_T\text{-III}} = 1/2\pi R_3C_3$ and other at $f_{p2\_T\text{-III}} = (C_1+C_2)/2\pi R_3C_3$. The zeros are at $f_{z1\_T\text{-III}} = 1/2\pi R_2C_1$ and $f_{z2\_T\text{-III}} = 1/2\pi(R_1+R_3)C_3$, respectively. The two gains of controller network are $K_{1\_T\text{-III}} = R_2/R_1$ and $K_{2\_T\text{-III}} = R_2(R_1+R_3)/R_1R_3$. Now the two zeros have been considered at the same point and similarly the two poles are assumed the same point. So, the *double pole* and the *double zero* have been located at $\omega_{z1\_T\text{-III}} = \omega_{z2\_T\text{-III}} = \omega_{z1,2\_T\text{-III}}$ and $\omega_{p1\_T\text{-III}} = \omega_{p2\_T\text{-III}} = \omega_{p1,2\_T\text{-III}}$

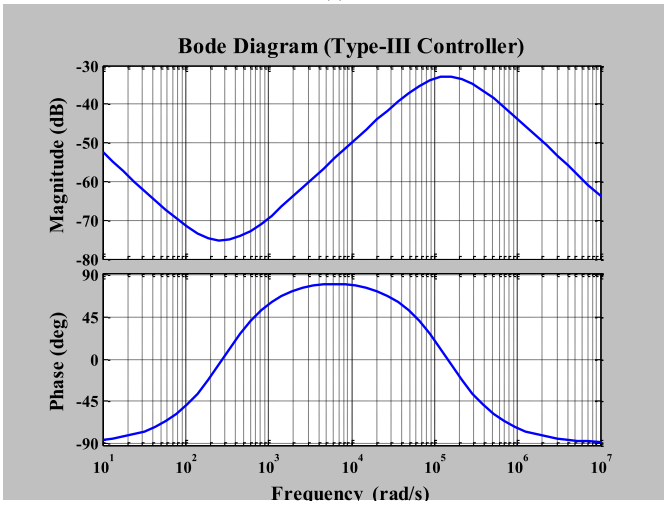
$$T_{c\_T\text{-III}}(s) = \frac{(1+s/\omega_{z1,2\_T\text{-III}})^2}{(s/\omega_{p0\_T\text{-III}})(1+s/\omega_{p1,2\_T\text{-III}})^2}. \quad (6)$$

The magnitude and argument of the controller can be written as

$$|T_{c\_T\text{-III}}(j\omega)| = \frac{\left|1+j\frac{\omega}{\omega_{z1,2\_T\text{-III}}}\right|\left|1+j\frac{\omega}{\omega_{z1,2\_T\text{-III}}}\right|}{\left|j\frac{\omega}{\omega_{p0\_T\text{-III}}}\right|\left|1+j\frac{\omega}{\omega_{p1,2\_T\text{-III}}}\right|\left|1+j\frac{\omega}{\omega_{p1,2\_T\text{-III}}}\right|} \quad (7)$$



(a)



(b)

Fig. 4. (a) Circuit diagram of Type-III controller. (b) Bode diagram of Type-III controller.

and the phase angle equation is given as

$$\arg T_{c\_T\text{-III}}(j\omega) = 2\tan^{-1}(\omega/\omega_{z1,2\_T\text{-III}}) - 2\tan^{-1}(\omega/\omega_{p1,2\_T\text{-III}}) - \frac{\pi}{2}. \quad (8)$$

From the Bode plot [Fig. 4(b)], it can be observed that the pole–zero combinations of Type-III controller can provide maximum 180° *phase boost* by changing the locations of poles/zeros. The *maximum phase boost* may be obtained by taking the derivate of (8) with respect to frequency f.

Finally, the *maximum phase boost* can be obtained at the *geometric mean* of the double zero–double pole frequencies in Type-III controller

$$f_{\max\_T\text{-III}} = \sqrt{f_{z1,2\_T\text{-III}} \times f_{p1,2\_T\text{-III}}}. \quad (9)$$

This geometric mean frequency is considered as crossover frequency ($f_{c\_T\text{-III}}$) in the Type-III controller.

C. Derivation of 'k' in Type-III Controller

"k" is defined as the ratio of the double pole frequency to the double zero frequency in Type-III controller [38]. These poles–zeros combinations provide maximum *phase boost* 180° at the crossover frequency. The relation between "k" and the *phase boost* of this controller can be written as follows [38]–[40]:

$$k = \left\{\tan\left(\frac{\text{phase boost}}{4} + \frac{\pi}{4}\right)\right\}^2. \quad (10)$$

So, the double pole and double zero locations can be found as follows:

$$f_{p1,2\_T\text{-III}} = \sqrt{k} \times f_{c\_T\text{-III}} = \tan\left(\frac{\text{phase boost}}{4} + \frac{\pi}{4}\right) \times f_{c\_T\text{-III}} \quad (11)$$

and

$$f_{z1,2\_T\text{-III}} = \frac{f_{c\_T\text{-III}}}{\sqrt{k}} = f_{c\_T\text{-III}}/\tan\left(\frac{\text{phase boost}}{4} + \frac{\pi}{4}\right). \quad (12)$$

If the crossover frequency ($f_{c\_T\text{-III}}$) and necessary *phase boost* of the Type-III controller are known, the exact locations of the double-pole/double-zero may be found from (11) and (12).

D. Midband Gain Adjustment for the Controller

The controller of (5) may be described as follows:

$$T_{c\_T\text{-III}}(s) = \frac{s}{\omega_{z1\_T\text{-III}}} \times \frac{(1+\omega_{z1\_T\text{-III}}/s)(1+s/\omega_{z2\_T\text{-III}})}{(s/\omega_{p0\_T\text{-III}})(1+s/\omega_{p1\_T\text{-III}})(1+s/\omega_{p2\_T\text{-III}})} = G_{o\_T\text{-III}}\frac{(1+\omega_{z1\_T\text{-III}}/s)(1+s/\omega_{z2\_T\text{-III}})}{(1+s/\omega_{p1\_T\text{-III}})(1+s/\omega_{p2\_T\text{-III}})}. \quad (13)$$

Here, $G_{o\_T\text{-III}}$ is known as *midband gain* and $G_{o\_T\text{-III}} = \omega_{p0\_T\text{-III}}/\omega_{z1\_T\text{-III}}$. The value of $\omega_{p0\_T\text{-III}}$ depends upon the required gain/attenuation at crossover frequency.

Now

$$G_{o\_T\text{-III}} = G_{T\text{-III}}\frac{\sqrt{1+\left(\frac{\omega_{c\_T\text{-III}}}{\omega_{p1\_T\text{-III}}}\right)^2}\sqrt{1+\left(\frac{\omega_{c\_T\text{-III}}}{\omega_{p2\_T\text{-III}}}\right)^2}}{\sqrt{1+\left(\frac{\omega_{z1\_T\text{-III}}}{\omega_{c\_T\text{-III}}}\right)^2}\sqrt{1+\left(\frac{\omega_{c\_T\text{-III}}}{\omega_{z2\_T\text{-III}}}\right)^2}} \quad (14)$$

where $G_{T\text{-III}}$ is an *assumed gain* at crossover frequency $f_{c\_T\text{-III}}$

$$\omega_{po\_T\text{-III}} = G_{T\text{-III}} \times \omega_{z1\_T\text{-III}} \times \frac{\sqrt{1+\left(\frac{\omega_{c\_T\text{-III}}}{\omega_{p1\_T\text{-III}}}\right)^2}\sqrt{1+\left(\frac{\omega_{c\_T\text{-III}}}{\omega_{p2\_T\text{-III}}}\right)^2}}{\sqrt{1+\left(\frac{\omega_{z1\_T\text{-III}}}{\omega_{c\_T\text{-III}}}\right)^2}\sqrt{1+\left(\frac{\omega_{c\_T\text{-III}}}{\omega_{z2\_T\text{-III}}}\right)^2}}. \quad (15)$$

If double coincident poles/zeros pair has been considered, the formula becomes

$$\omega_{p0\_T\text{-III}} = G_{T\text{-III}}\frac{\omega_{z1,2\_T\text{-III}}\left[\omega_{p1,2\_T\text{-III}}^2 + \omega_{c\_T\text{-III}}^2\right]}{\omega_{p1,2\_\text{III}}^2\sqrt{\left(\frac{\omega_{z1,2\_T\text{-III}}}{\omega_{c\_T\text{-III}}}\right)^2+1}\sqrt{\left(\frac{\omega_{c\_T\text{-III}}}{\omega_{z1,2\_T\text{-III}}}\right)^2+1}}. \quad (16)$$

E. Design Example of Type-III Controller

Let us assume a power supply that has a gain deficit of −10 dB at a 1-kHz selected crossover frequency. The necessary *phase boost* is 170°. From (11) and (12), the position of the double pole will be as follows:

$$f_{p1,2\_T\text{-III}} = \tan\left(\frac{\text{phase boost}}{4} + \frac{\pi}{4}\right) \times f_{c\_T\text{-III}} = \tan\left(\frac{170^{\text{o}}}{4} + 45^{\text{o}}\right) \times 1000 = 22.904 \text{ kHz}. \quad (17)$$

The double zero is placed at

$$f_{z1,2\_T\text{-III}} = f_{c\_T\text{-III}} \Big/ \tan\left(\frac{\text{phase boost}}{4} + \frac{\pi}{4}\right) = 1000 \Big/ \tan\left(\frac{170^{\text{o}}}{4} + 45^{\text{o}}\right) = 43.6609 \text{ Hz}. \quad (18)$$

The gain $G_{T\text{-III}}$ at 1 kHz has chosen −10 dB. So, the position of the 0-dB crossover pole at

$$f_{p0\_T\text{-III}} = G_{T\text{-III}} \times \frac{f_{z1\_T\text{-III}}\left(f_{p1,2\_T\text{-III}}^2 + f_{c\_T\text{-III}}^2\right)}{f_{p1,2\_T\text{-III}}^2 \sqrt{\left(\frac{f_{z1,2\_T\text{-III}}}{f_{c\_T\text{-III}}}\right)^2 + 1} \sqrt{\left(\frac{f_{c\_T\text{-III}}}{f_{z1,2\_T\text{-III}}}\right)^2 + 1}} = 6.03 \text{ Hz}. \quad (19)$$

So, the final transfer function of the classical Type-III controller after adjusting the gain is given by

$$\frac{6.552 \times 10^3 (s + 274.3)^2}{s(s + 1.439 \times 10^5)^2}.$$

The values of different components of Type-III controller network [from Fig. 4(a)] can be calculated as follows.

Let us assume, $R_1 = 10$ kΩ, $R_2 = 33$ kΩ and $R_3 = 1.5$ kΩ

$$\text{So, } C_1 = \frac{1}{R_2 * 274.3} = \frac{1}{33 * 10^3 * 274.3} = 0.1105 * 10^{-6} \text{ F}. \quad (20)$$

Now, put the value of R_2 and C_1 in $((C_1 + C_2)/(R_2 * C_1 * C_2)) = 1.439 * 10^5$ or

$$C_2 = 210.9865 * 10^{-12} \text{ F} \quad (21)$$

and $(1/((R_1 + R_3)C_3)) = 274.3$ or

$$C_3 = \frac{1}{(10 + 1.5) * 10^3 * 274.3} = 0.317 * 10^{-6} \text{ F}. \quad (22)$$

The values of passive components of the practical Type-III controller are given as: $R_1 = 10$ kΩ, $R_2 = 33$ kΩ, $R_3 = 1.5$ kΩ, $C_1 = 0.12$ μF, $C_2 = 220$ pF, and $C_3 = 0.33$ μF. Here, the standard capacitance values (near to designed values) are considered.

IV. Design of PSO-Based Optimized Type-III Controller

A. Overview Particle Swarm Optimization

PSO is an evolutionary algorithm (technique) that optimizes the continuous or discrete, linear or nonlinear, constrained or unconstrained, nondifferentiable functions by iteratively trying to improve the solutions for different parameter values [39]. The PSO is based on the behavior of a colony of living things, such as swarm of insects, flock of birds, or school of fish. The insects, fishes, animals, especially birds, and so on, always travel in a group without crashing each other from their group members by adjusting their positions and velocities from using their group information. Because this method reduces individual effort for searching the food, shelter, and so on. In this paper, PSO algorithm is used to design the optimal Type-III controller that has been implemented for the overall improvement of BC and IBC.

TABLE II
PARAMETERS OF PSO METHOD

Sl. No.	Parameter	Value
1.	Cognitive Constant (C_1)	1.44495
2.	Group Constant (C_2)	1.44495
3.	Number of Particles(n_p)	50
4.	Number of Iteration (t_{max})	100

B. Fitness Function for PSO

To obtain the optimum performance, the *fitness function* with typical *performance criteria* is the first step for designing the PSO-based *optimized Type-III controller* with desired specifications and constraints under input step signal. Some important output specifications in the time domain are *overshoot*, *rise time*, *settling time*, and *steady-state error*. The minimum value of this fitness function/objective function corresponds to the optimum set of parameter values. The selection of fitness functions is the most crucial step in applying PSO. Generally, there are four kinds of *performance criteria*, such as the integral absolute error, the integral of squared error, the integral of time weighted squared error, and the integral of time weighted absolute error (ITAE) [39]. The ITAE performance criterion provides the fastest response with small overshoot for a class of optimization techniques, so ITAE is chosen as a *fitness function* in this simulation study and is expressed as

$$\text{fit}(t) = \int_0^{\tau} t|e(t)|dt \quad (23)$$

where the upper limit τ is chosen as steady-state value.

C. Computational Implementation of PSO

A concise idea about the PSO algorithm has been described here. The position of the qth agent among n_p total number of agent vectors (population) is defined as

$$Y_q = \left(Y_q^1, Y_q^2, Y_q^3, \ldots Y_q^d, \ldots Y_q^n\right) \quad \text{for } q = 1, 2, \ldots, n_p \quad (24)$$

where Y_q^d represents the position of qth particle vector in the dth dimension and n is the total number of dimensions.

In this paper, each particle vector of the population n_p denotes five parameters or dimensions for Type-III controller (Y_q^1 = controller gain, Y_q^2 = first zero location, Y_q^3 = second zero location, Y_q^4 = first pole location, and Y_q^5 = second pole location).

The velocity vector along each dimension for the particle vector is represented as

$$v_q = \left(v_q^1, v_q^2, v_q^3, \ldots, v_q^d, \ldots, v_q^n\right). \quad (25)$$

TABLE III
COMPARITIVE STUDY OF CLOSED-LOOP PERFORMANCES OF BC AND TWO-PHASE IBC

Specifications	Classical TYPE-III Controller (*k*-factor approach)		Optimal TYPE-III Controller (PSO approach)	
	Boost Converter	Interleaved Boost Converter	Boost Converter	Interleaved Boost Converter
Maximum Overshoot (M_p)	0 %	0 %	0 %	0 %
Rise Time (t_r)	0.00386 sec	0.00183sec	0.00368 sec	0.00171sec
Settling Time (t_s)	0.00686 sec	0.00322 sec	0.00654 sec	0.00286 sec
Steady-State Error (E_{ss})	0	0	0	0
Phase Margin (PM)	67.3°	88.1°	68.6°	90.2°
Gain Crossover Frequency (GCF)	5720 rad/sec	6490 rad/sec	5980 rad/sec	6790 rad/sec
Gain Margin (GM)	12.2 dB	13.9 dB	13.1 dB	15.4 dB
Phase Crossover Frequency (PCF)	15700 rad/sec	68700 rad/sec	23800 rad/sec	88600 rad/sec
Controller Gain (G_{o_III})	6.552×10^3	6.552×10^3	0.25918×10^3	0.25918×10^3
Controller Transfer Function (T_{c_III})	$\frac{6.552\times10^3(s+274.3)^2}{s(s+1.439\times10^5)^2}$	$\frac{6.552\times10^3(s+274.3)^2}{s(s+1.439\times10^5)^2}$	$\frac{0.25918\times10^3(s^2+1090s+4.98\times10^5)}{s(s+1.83\times10^5)(s+2.83\times10^4)}$	$\frac{0.25918\times10^3(s^2+1090s+4.98\times10^5)}{s(s+1.83\times10^5)(s+2.83\times10^4)}$
Closed-Loop Stability	Stable	Stable	Stable	Stable

Each particle also maintains a memory of its previous best position which is known as personal best position and denoted as $p$best

$$p\text{best}_q = \left(p\text{best}_q^1, p\text{best}_q^2, p\text{best}_q^3, \ldots, p\text{best}_q^d, \ldots p\text{best}_q^n\right). \tag{26}$$

The global best position which has been found by the swarm so far is given as

$$g\text{best} = \left(g\text{best}^1, g\text{best}^2, g\text{best}^3, \ldots, g\text{best}^d, \ldots, g\text{best}^n\right). \tag{27}$$

The global best positions and the individual's previous best positions are associated with the particle velocity vector along each dimension and that velocity vector is then used to calculate a new particle position vector. The portion of the velocity adjustment influenced by the individual's previous best ($p\text{best}_q^d$) is known as *cognitive part*, and the portion influenced by the global best ($g\text{best}^d$) is known as *social component*. The formulas of the *velocity* and *position* in PSO, which is introduced by Eberhart and Kennedy [41] and Kennedy [43], are expressed as

$$v_q^d(t+1) = v_q^d(t) + C_1 \times \text{rand}_1() \times \left(p\text{best}_q^d(t) - Y_q^d(t)\right) + C_2 \times \text{rand}_2() \times \left(g\text{best}^d(t) - Y_q^d(t)\right) \tag{28}$$

$$Y_q^d(t+1) = Y_q^d(t) + v_q^d(t+1) \tag{29}$$

where C_1 and C_2 are known as learning rate constant. $t_{\max}$ is the maximum number of iterations, t is the current iteration number and $\text{rand}_1()$ and $\text{rand}_2()$ are uniformly distributed random numbers in the range [0, 1]. Here, C_1 and C_2 are set to the same values to give equal weights to the cognitive and social parts. The parameters C_1 and C_2 denote the relative importance of the memory (position) of the particle itself to the memory (position) of the swarm. The flowchart of the PSO algorithm is given in Fig. 5.

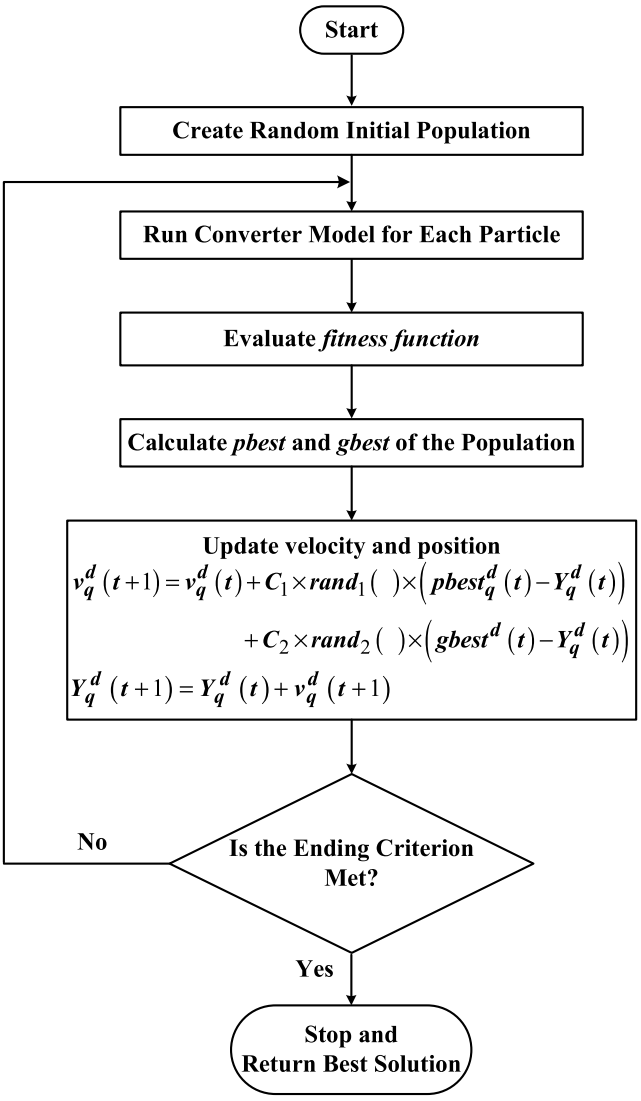
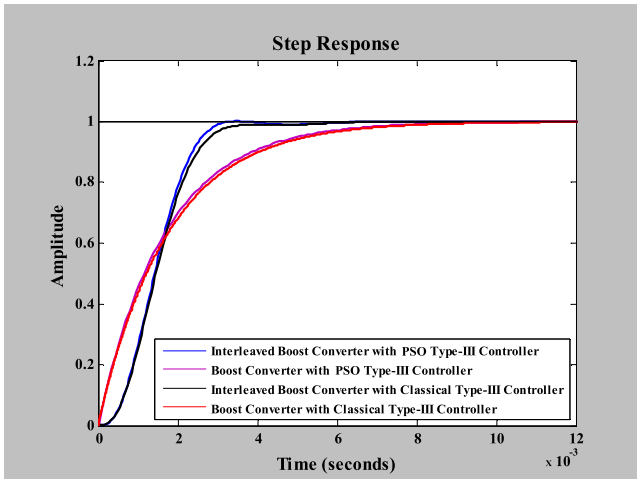


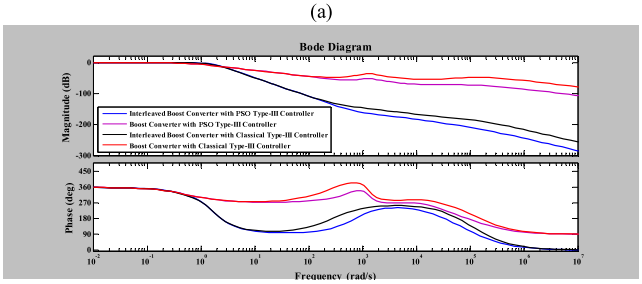
Fig. 5. Flowchart of the PSO process.

D. Optimization Specifications

The parameters of the Type-III controllers are to be optimized by using the PSO-based optimization technique. There are actually six parameters for Type-III controller, but for optimization five parameters, namely, one dc gain, one pair of zeros, and one pair of poles have been considered.



(a)



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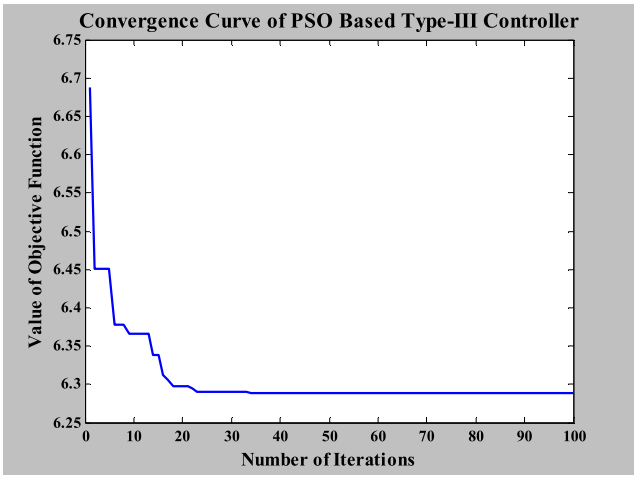


(c)

Fig. 6. (a) Closed-loop step responses. (b) Closed-loop Bode diagram of BC and two-phase IBC with Type-III controllers. (c) Convergence curves of fitness function (fit(t)) for optimized Type-III controller.

The pole at origin has not been considered because of its fixed location. The flowchart of the optimization process is given in Fig. 5. The routine for PSO has been written in MATLAB (version R2011a). The values for the PSO parameters are given in Table II.

The transfer function of the PSO-based optimal Type-III controller for IBC is given by

$$T_{c\_T\text{-III}}(s) = \frac{0.25918 \times 10^3 (s^2 + 1090s + 4.98 \times 10^5)}{s(s + 1.83 \times 10^5)(s + 2.83 \times 10^4)}.$$

V. Simulation Results and Discussion

Extensive simulation has been carried out to find the dynamic performances of BC and IBC with classical and optimal Type-III controller under MATLAB/SIMULINK environment. Here, the objective is to develop a suitable optimal Type-III controller for closed-loop BC and IBC, so that superior dynamic performance will be achieved.

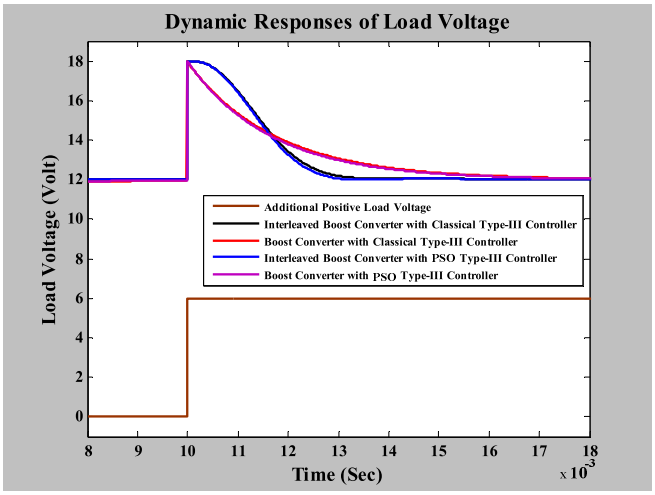
The dynamic performances in terms of step and frequency response of the dc–dc BC and IBC with classical and optimal Type-III controllers have been reported in Fig. 6(a) and (b) and in Table III. It is clear that IBC with PSO-based optimal Type-III controller provides better dynamic response than BC. The step response of IBC with optimized Type-III controller exhibits the fastest response (rise time = 0.00171 s) with zero overshoot and zero steady-state error. It is to be mentioned that the "*k-factor*" approach is a standard method for the designing of classical Type-III controller and in the present case it worked well for both closed-loop IBC and BC. In the frequency domain analysis, it is observed that PSO-based Type-III controller provides maximum phase margin (90.2°), gain margin (15.4 dB), *Gain Crossover Frequency (GCF)* (6790 rad/s), and *Phase Crossover Frequency (PCF)* (88 600 rad/s). Fig. 6(c) shows the plot of minimum values of the fitness function (fit(t)) versus number of iterations for Type-III controller for IBC.

The load regulations of the proposed converters have been observed by applying an additional ±50% load voltage [Fig. 7(a) and (b)]. Both BC and IBC have maintained the load regulation with the proposed classical and optimized Type-III controllers and try to keep the load voltage fixed at 12 V. The initial transients are shown due to the sudden changes of load voltages, but output voltage has reached immediately to its steady-state value of 12 V. Though the load regulations have been maintained by both the converters, the PSO-based optimal Type-III controller with IBC has shown the best closed-loop dynamics (zero overshoot and least settling time) than the classical/optimal Type-III controller with BC. The tracking performances of the load voltages of BC and IBC are observed by applying an additional ±50% of reference voltage (V_{ref}) [Fig. 7(c) and (d)]. The IBC with PSO-based optimal Type-III controller shows [Fig. 7(c) and (d)] the best tracking performance than the performance of BC with optimal controller. The load voltage of IBC with optimal controller has perfectly tracked the reference voltage (V_{ref}) and settles down quickly maintaining zero steady-state error. So, it may be concluded from simulation results that IBC with optimal controller provides satisfactory tracking performance and exhibits good load regulation in closed loop. Fig. 7(e) shows the simulated response of input current, inductor currents i_{L1} and i_{L2}, gate pulse for S_1, and gate pulse for S_2 during steady state. It is clear from Fig. 7(e) that the two inductor currents as well as two gate pulses are at 180° out of phase to each other. The input current which is the resultant of two inductor currents consists of smaller ripple compared with individual inductor current.

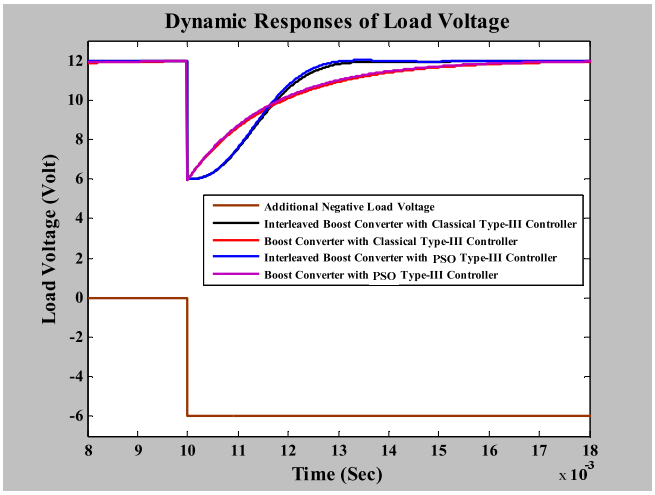
VI. Experimental Results and Discussion

A. Description of Experimental Details

The closed-loop two-phase IBC and conventional boost converter has been implemented with the designed classical and optimal controllers in the laboratory. The overall circuit



(a)



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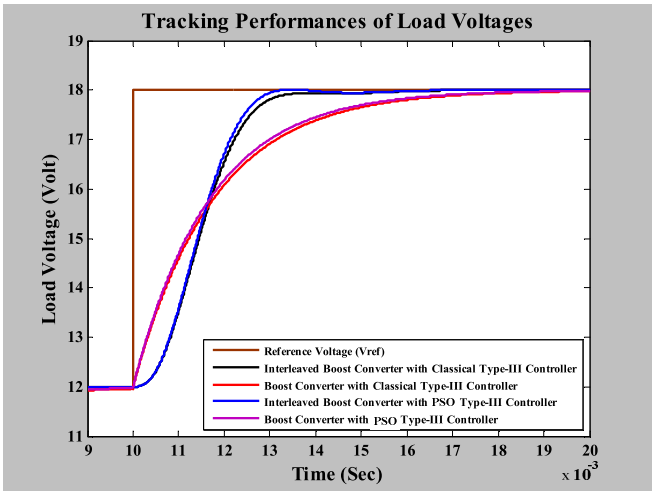

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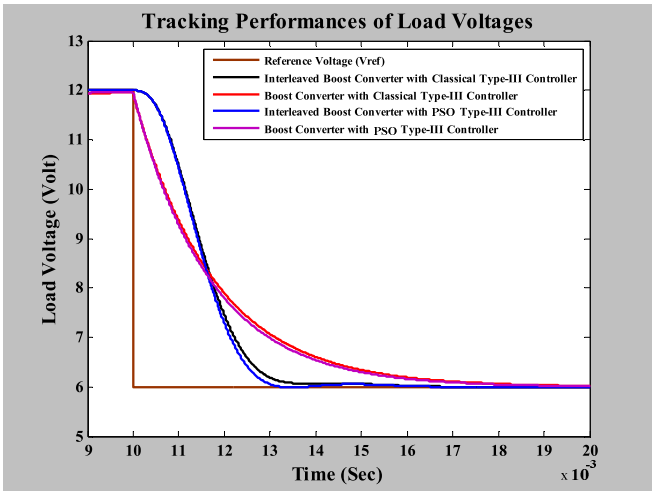
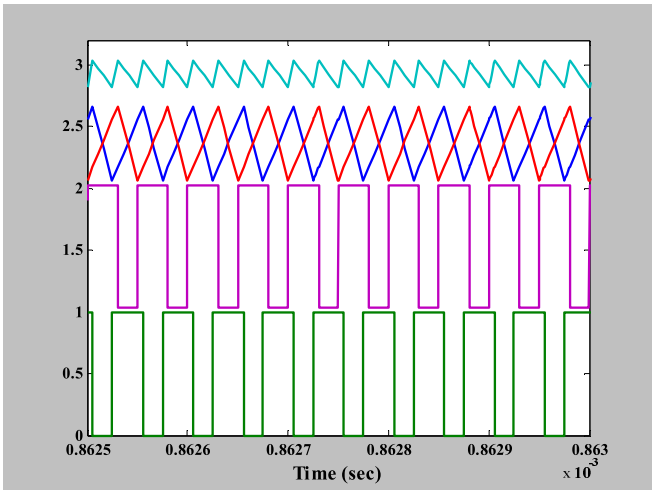


(d)



(e)

Fig. 7. (a) and (b) Dynamic response of load voltage by applying an additional ±50% load voltage. (c) and (d) Dynamic response of load voltage by applying an additional ±50% reference voltage (V_{ref}). (e) Steady-state waveform of input current, two-phase inductor currents, and gate pulses of IBC.

diagram of the closed-loop system of IBC is shown in Fig. 8. The power circuit consists of input dc power supply, two MOSFETs (IRFP450), two fast recovery diodes (MUR460), two filter inductors of 275 μH, an electrolytic capacitor of 470 μF, and a 50 W variable load resistance. The inductor has been designed and fabricated based on fundamental principle. In the control circuit, IC 8038 is used as a function generator, which generates triangular waveform of 20 kHz with some

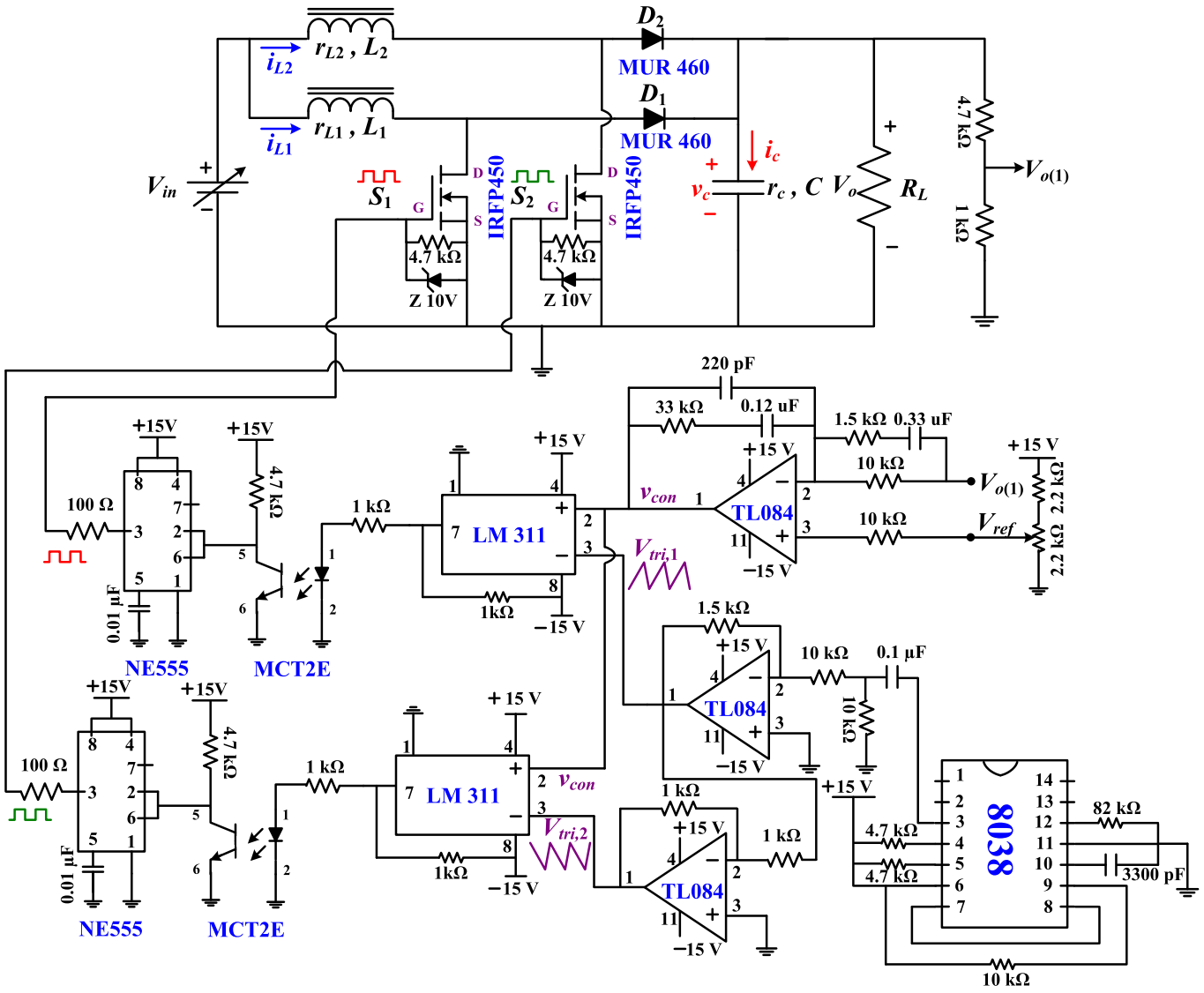
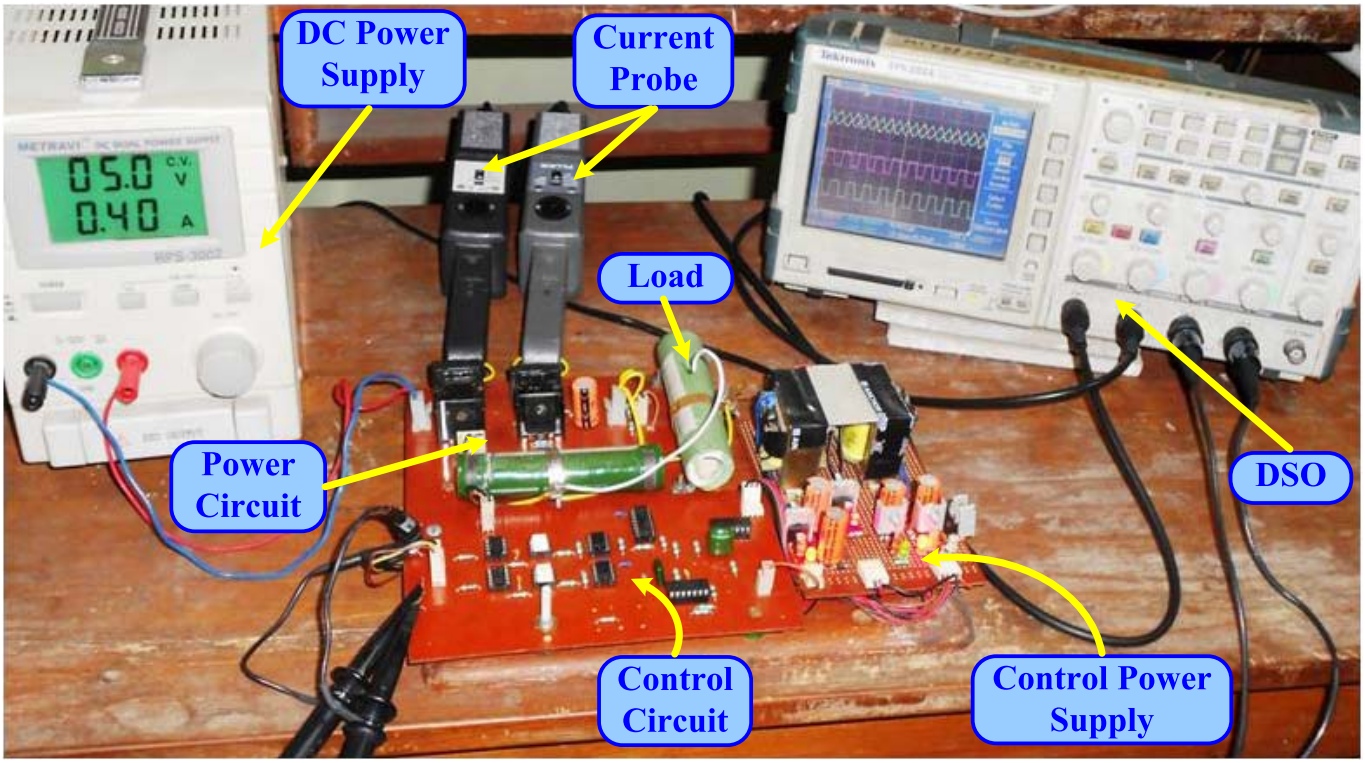


Fig. 8. Circuit diagram of voltage-mode controlled two-phase IBC.

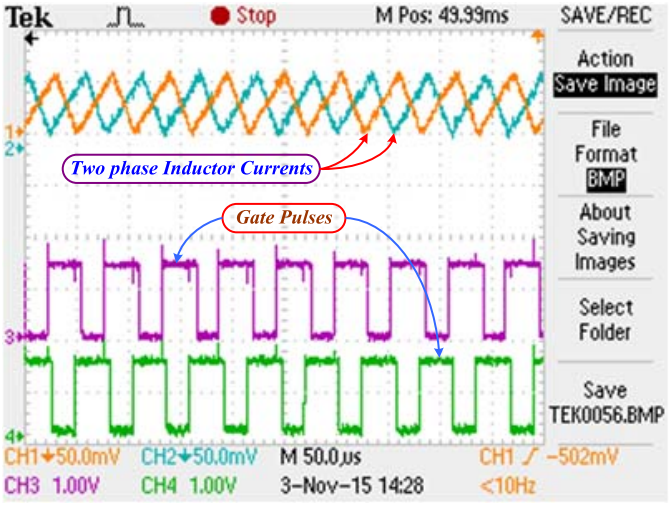
dc-biased voltage. This essentially means the switching frequency of the IBC will be 20 kHz. An *RC* circuit eliminates the dc-biased voltage and generates positive and negative peak of triangular waveform. Conditioned triangular waveform is feeding to an inverting op-amp amplifier. Another inverting op-amp amplifier is used for 180° phase shift of the triangular waveform. Two LM311 ICs are used as voltage comparator, one comparing control signal (v_{con}) output of optimal Type-III controller with normal triangular waveform ($V_{\text{tri},1}$) and generating PWM signal for S_2 and another IC comparing control signal (v_{con}) with 180° phase shifted triangular waveform ($V_{\text{tri},2}$) and generating PWM signal for S_1. These PWM signals are passed through optoisolators (MCT2E) and astable-multivibrators (NE555) before driving MOSFET switches (S_1 and S_2).

B. Experimental Results

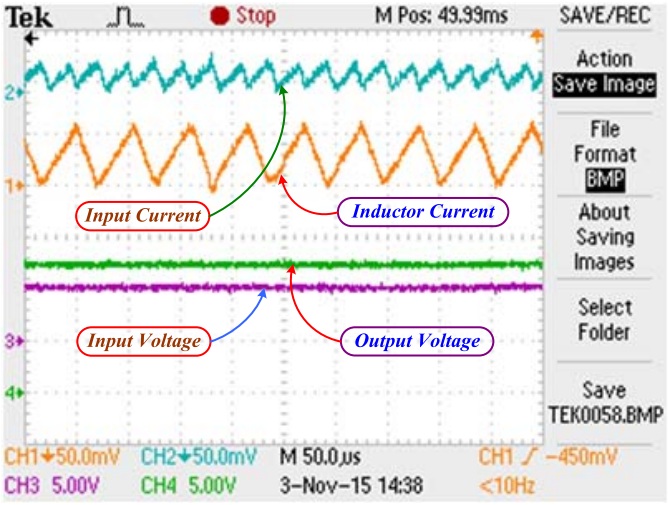
A laboratory scale prototype of two-phase IBC has been designed and fabricated in PCB. The overall experimental setup of the system is shown in Fig. 9(a). The steady-state waveforms of two-phase inductor currents, input current, gate pulses for MOSFETs, input voltage, and output voltage are shown in Fig. 9(b) and (c). Like simulated results, the two inductor currents as well as two gate pulses are at 180° out of phase to each other [Fig. 9(b)] and the input current which is the resultant of two inductor currents consists of smaller ripple compared with individual inductor current [Fig. 9(c)]. The nominal input voltage and output voltage of the IBC is 5 and 12 V, respectively. From the simulation results (Fig. 7), it is clear that for the given IBC, PSO-based optimal Type-III controller has shown the best closed-loop performance and the *k-factor*-based classical Type-III controller with BC produces relatively the worst result while comparing the converter performances with different controllers. Both classical and optimal Type-III controllers have been utilized experimentally for the closed-loop control of the proposed IBC and BC. The practical output voltage responses of IBC and BC with PSO Type-III controller with positive, negative,



(a)



(b)



(c)

Fig. 9. (a) Experimental setup for laboratory prototype. (b) and (c) Experimental results of steady-state wave forms of two-phase inductor currents, gate pulses for MOSFETs, input current, single inductor current, input supply voltage, and output voltage.

and repetitive step changes in load voltage have been shown in Figs. 10 and 11, respectively. It is clear that in both the cases, the output voltage responses exhibit the fast response with producing little overshoot. But in the case of IBC with PSO-based optimal Type-III controller, it shows the fastest dynamic response compared with the BC with PSO Type-III controller. The *k-factor*-based classical Type-III controller with BC shows the worst performance with large overshoot [Fig. 11(a)–(c)]. The dynamics of output voltage, input current, and inductor current are also observed. The currents are measured by Fluke and Techtronic's made current probes with a scale of 100 mV = 1 A. From Figs. 10 and 11, it is clear that the PSO-based optimal Type-III controller with IBC has shown the best dynamic performance compared with the BC with optimal Type-III controller. The comparative dynamic performance between BC and IBC is presented in Table IV.

VII. Comparative Study Between Boost and Interleaved Boost Converters

In this section, a comparative study between BC and IBC is presented based on the ripples of input current and output voltage from the experimental results (Figs. 10 and 11). It is clear that the ripple content in the input current, inductor current, and output voltage is less in IBC irrespective of any

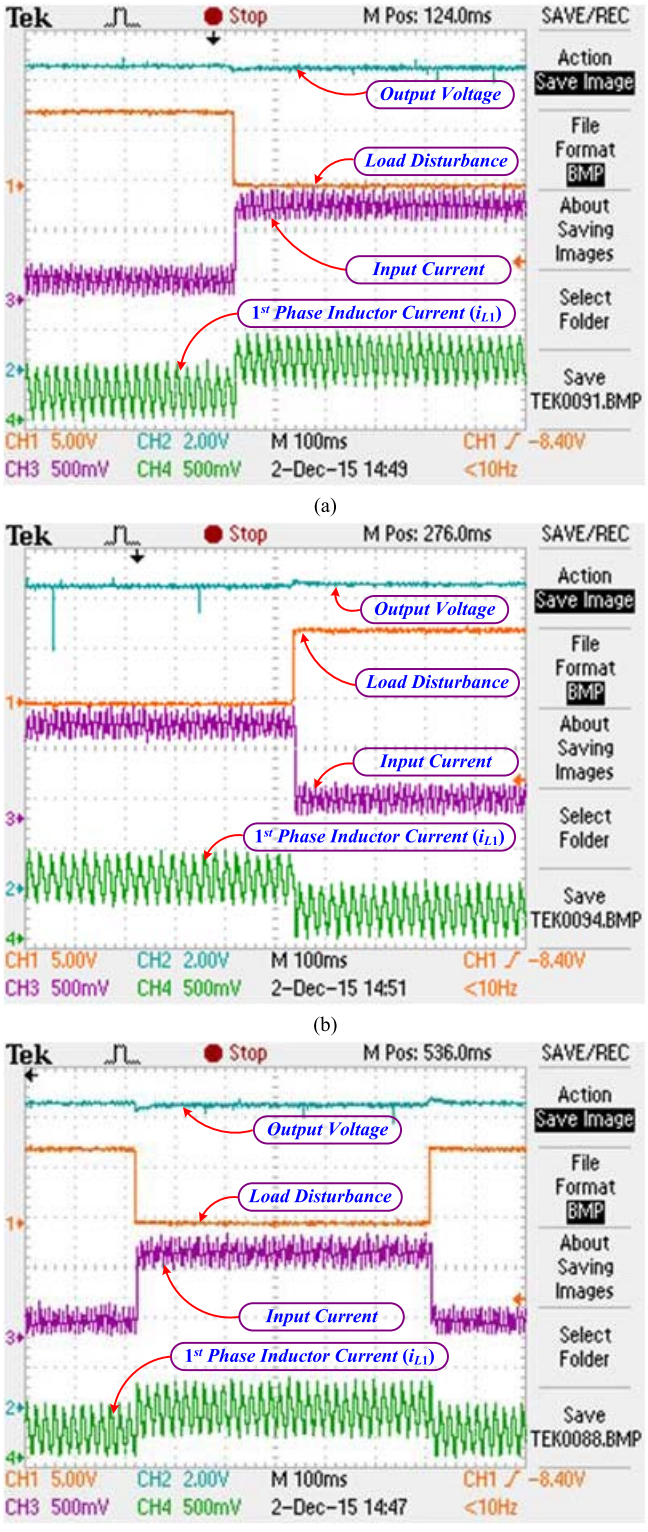


Fig. 10. Transient response of load voltages with (a) negative, (b) positive, and (c) repetitive step load disturbance of IBC with PSO Type-III controller [Ch1: load disturbance. Ch2: output voltage. Ch3: input current. Ch4: inductor current].

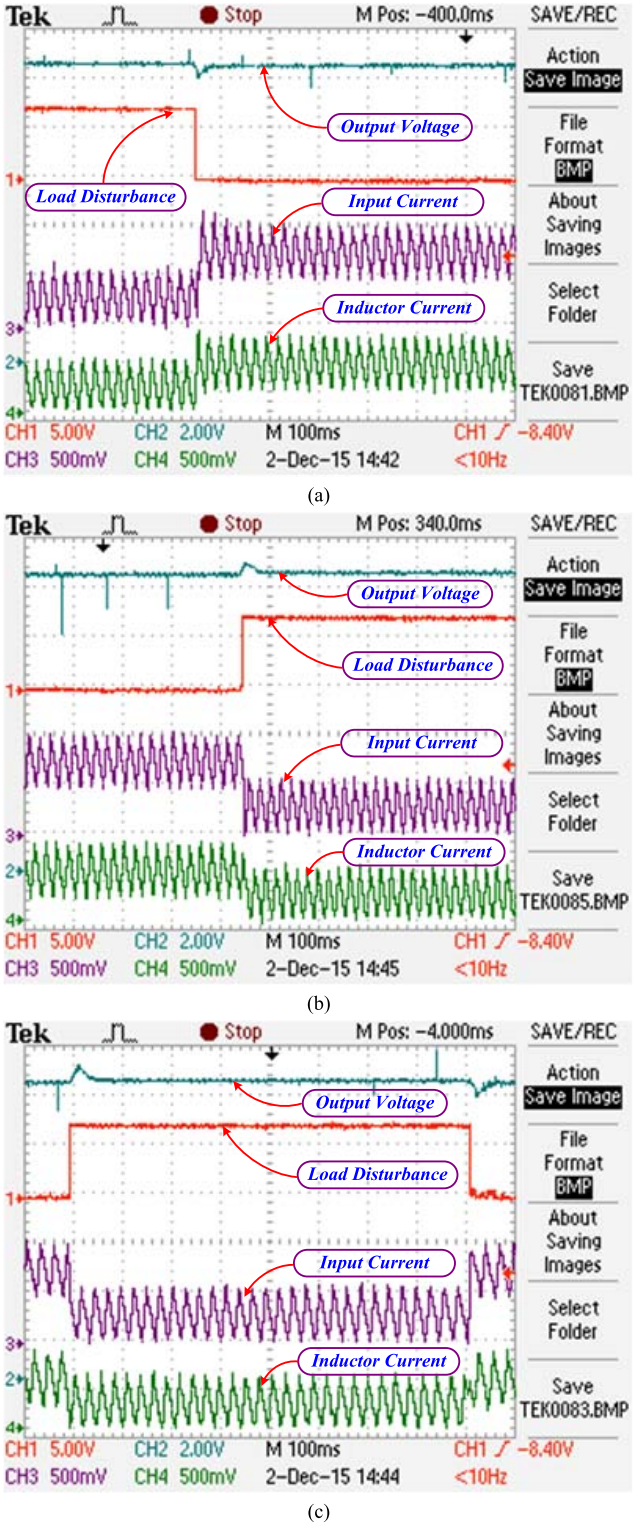


Fig. 11. Transient response of load voltages with (a) negative, (b) positive, and (c) repetitive step load disturbance of BC with *k-factor*-based classical Type-III controller [Ch1: load disturbance. Ch2: output voltage. Ch3: input current. Ch4: inverted inductor current].

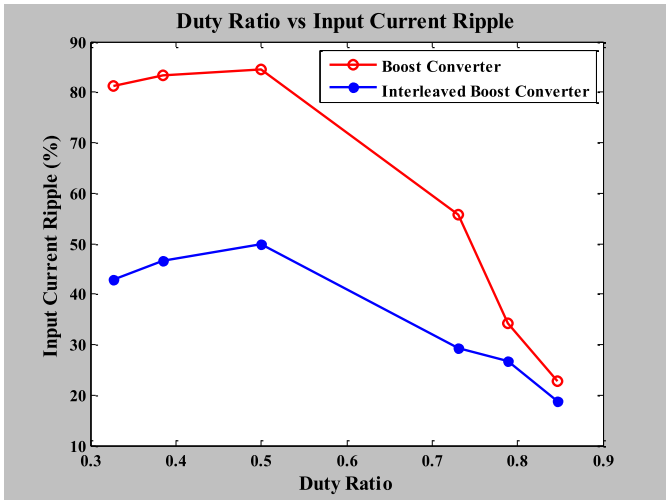
duty cycle. Table V also shows that IBC produces less ripple in input current and output voltage in comparison with the normal BC. The input current ripple and the output voltage ripple of BC and IBC are determined from the experimental waveforms and are plotted against duty cycle ratios in Fig. 12(a) and (b). The ripple content in input current for both IBC and BC is reaching maximum at 50% duty cycle and after that percentage ripple is reduced, but output voltage

TABLE IV
COMPARITIVE CLOSED-LOOP PERFORMANCES OF BC AND IBC (EXPERIMENTAL STUDY)

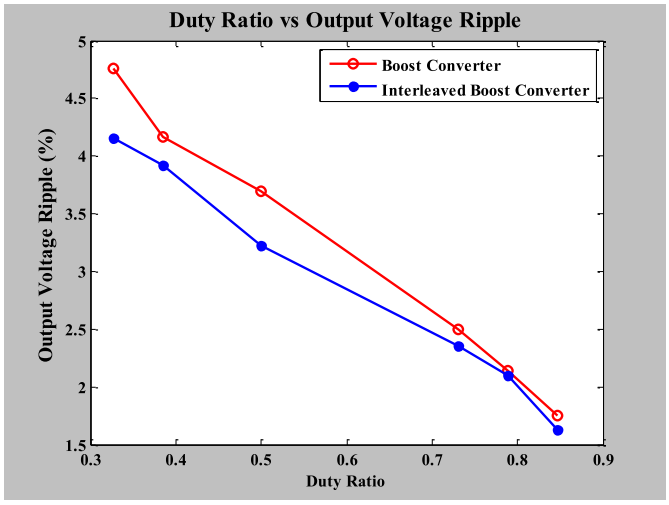
SPECIFICATIONS	BOOST CONVERTER	INTERLEAVED BOOST CONVERTER
Maximum Overshoot (M_p)	6.67 %	3.33 %
Rise Time (t_r)	0.025 sec	0.01 sec
Settling Time (t_s)	0.04 sec	0.02 sec

TABLE V
PERCENTAGE RIPPLE VERSUS DUTY RATIO FOR BC AND IBC

	DUTY RATIO											
	32.75%		38.46%		50 %		71.15%		78.84%		84.615%	
Parameters	BC	IBC	BC	IBC	BC	IBC	BC	IBC	BC	IBC	BC	IBC
Input Current Ripple	81.25 %	42.85 %	83.33 %	46.66 %	84.60 %	50 %	55.81 %	29.41 %	34.32 %	26.66 %	22.85 %	18.86 %
Output Voltage Ripple	4.76 %	4.16 %	4.167 %	3.92 %	3.7 %	3.22 %	2.5 %	2.35 %	2.14 %	2.1 %	1.75 %	1.63 %



(a)



(b)

Fig. 12. Comparative study between BC and two-phase IBC. (a) Input current ripple versus duty ratio. (b) Output voltage ripple versus duty ratio.

ripple is reduced monotonically with the duty ratio. At 50% duty cycle, there is almost 13% reduction of ripple in output voltage of IBC than normal BC.

VIII. CONCLUSION

In this paper, the design and implementations of optimal Type-III controller-based two-phase IBC have been demonstrated. The controller has been designed initially by using "*k-factor*" approach, and then the parameters of controller have been tuned by the PSO-based optimization technique for obtaining better stability and performance. The closed-loop performances and the comparative analysis for IBC and BC have been studied in both simulation and experimentation. It is observed that the ripple content in the input current, inductor current, and output voltage is less in IBC compared with the conventional BC irrespective of any duty cycle.

It may be concluded that the optimized Type-III controller with IBC exhibits the best closed-loop performance, the highest system bandwidth and the largest margin of stability. So, PSO-based optimal Type-III controller may be used for the design and implementation of SMPS utilizing IBC to improve the overall closed-loop stability and performance. The proposed control algorithm may be applicable for higher rated power converters for different applications such as hybrid electrical vehicles, SVG, HVDC applications, MES, and so on. The proposed IBC converter having very fast transient response and absence of high frequency ripple may be applicable for maximum power extraction from SPV panels. Here, it is to be mentioned that PSO-based optimal Type-III control for IBC is newly introduced in this paper and not been reported earlier in any literature.

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