LETTER

A Low Noise CMOS Low Dropout Regulator with an Area-Efficient Bandgap Reference

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SUMMARY   In a low dropout (LDO) linear regulator whose reference voltage is supplied by a bandgap reference, double stacked diodes increase the effective junction area ratio in the bandgap reference, which significantly lowers the output spectral noise of the LDO. A low noise LDO with the area-efficient bandgap reference is implemented in $0.18\,\mu$m CMOS. An effective diode area ratio of 105 is obtained while the actual silicon area is saved by a factor of 4.77. As a result, a remarkably low output noise of $186\,$nV/sqrt(Hz) is achieved at 1 kHz. Moreover, the dropout voltage, line regulation, and load regulation of the LDO are measured to be 0.3 V, 0.04%/V, and 0.46%, respectively.
key words: *low dropout regulator (LDO), bandgap reference, CMOS*

1.   Introduction

System on chip (SoC) technology is a recent trend to fully integrate the digital, analog, and RF blocks on a single chip. For the SoC, power management needs to be more distributed for efficient power saving. Thus, the local implementations of regulators and reference blocks on a chip are increasingly indispensable [1]. Conventionally, major design issues of LDO include stability, fast transient response, high power supply rejection, frequency compensation with on-chip capacitors etc. [1]–[4]. Meanwhile, it is found that when LDO and reference generator are embedded in RFICs, the output spectral noise of the LDO becomes one of the critical performance parameters as well. It is because the output spectral noise will impose a direct impact on the noise performances of the accompanying RFIC blocks. For example, it would degrade the noise figure in a receiver, the output noise level in a transmitter, or the phase noise in a phase locked loop. Wu et al. had demonstrated the significant effect of the LDO on the VCO phase noise in their low phase noise VCO design [5].

On-chip LDO is typically accompanied by a precision reference voltage generator such as a bandgap voltage reference (BGR). In this structure, the output noise of the LDO is typically dominated by the BGR, and BGR typically requires extremely large diode-connected bipolar junction transistors (BJTs) for very low output noise. In this work, we employ stacked diodes to increase the effective area ratio in the BGR, and by using the area efficient BGR, a low noise

LDO is achieved.

2.   Output Noise Analysis of LDO

Figure 1 shows the general structure of the LDO and BGR. The output voltages V_{REF} and V_{OUT} of the BGR and LDO, respectively, are given by

$$V_{REF} = V_{BE3} + N\frac{R_2}{R_1}V_t \ln M \qquad (1)$$

$$V_{OUT} = V_{REF}\left(1 + \frac{R_4}{R_5}\right) \qquad (2)$$
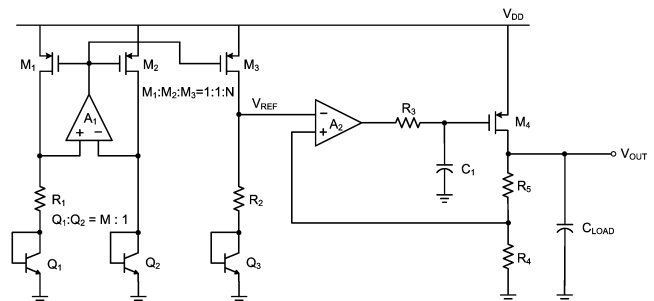
where V_t is the thermal voltage, V_{BE3} is the base-emitter junction voltage of Q_3, and other circuit parameters are noted in Fig. 1. The output noise at V_{OUT} is usually dominated by the op-amps A_1 and A_2, and simply expressed by

$$\bar{v}_{n,out}^2 \cong \left(1 + \frac{R_5}{R_4}\right)^2 \cdot \left[\left(\frac{R_2}{R_1}\right)^2 \cdot \bar{v}_{n,A_1}^2 + \bar{v}_{n,A_2}^2\right] \qquad (3)$$

where $\bar{v}_{n,A_i}^2$ is the input referred noise voltage of op-amp A_i. Assuming the op-amps A_1 and A_2 are identical and thus create the same level of output noise, the noise contribution by A_1 is usually greater than that by A_2 by a factor of R_2/R_1. Substituting for (R_2/R_1) in (3) from (1), the output noise is given by

$$\bar{v}_{n,out}^2 \cong \left(1 + \frac{R_5}{R_4}\right)^2 \cdot \left[\left(\frac{V_{REF} - V_{BE3}}{NV_t \ln M}\right)^2 \cdot \bar{v}_{n,A_1}^2 + \bar{v}_{n,A_2}^2\right] \quad (4)$$

From (4), it can be known that N and/or M must be increased in order to reduce the noise contributions from $v_{n,A1}$. Increasing N will directly lead to higher current consumption of the LDO. Thus, increasing M will be a more appro-

Fig. 1   General structure of low dropout regulator with bandgap voltage reference.

Fig. 2 Output spectral noise with respect to the diode area ratio.

Fig. 3 Transistor-level circuit schematic of the low dropout regulator with the bandgap reference.

Fig. 4 Chip micrograph.

priate approach for reducing the output noise. This relationship was also recognized in [5]. Since M is embedded in the logarithmic operator in (4), an exponential increase of M will only lead to a linear decrease of output noise. Such effects are confirmed though circuit simulations of a test LDO circuit designed in $0.18\,\mu$m CMOS. Figure 2 shows the simulated output noise voltages at V_{REF} and V_{OUT} with respect to M. Note that the difference between the BGR and LDO output noises is mainly due to the factor $(1 + R_5/R_4)$ as implied by (3), which is 1.5 in this design. As can be seen, M must be extremely large to get a low output noise voltage. In such relationship, unfortunately, the required M value easily becomes impractically high if we want a very low output noise.

Replacing the diodes Q_1 and Q_2 with double stacked diodes can increase the effective value of M while not consuming much actual silicon area. When the area ratios of the upper and lower diode pairs are M_1 and M_2, respectively, V_{REF} expression of (1) is modified to

$$V_{REF} = V_{BE3} + \frac{R_2}{R_1} V_T \ln(M_1 M_2) \tag{5}$$

Here, the effective area ratio becomes $M_1 \times M_2$ while the actually consumed area is only $M_1 + M_2$. Thus, an area saving factor S_A can be defined as

$$S_A = \frac{M_1 M_2}{M_1 + M_2} \tag{6}$$

For example, if M_1 and M_2 are set to 10, then the overall effective area ratio M becomes 100 while the actually consumed area is only 20. Thus, the diode area is saved by a factor of 5. This means that by using the stacked diode in the BGR, we can realize a very high value of M without consuming much actual silicon area, and as a result, we can significantly reduce the output noise of the LDO.

3. Circuit Design and Measured Results

A 1.8 V low noise LDO regulator is designed for a $0.18\,\mu$m CMOS direct conversion transmitter that is developed for cognitive radio applications [6]. The LDO is to provide a 1.8 V s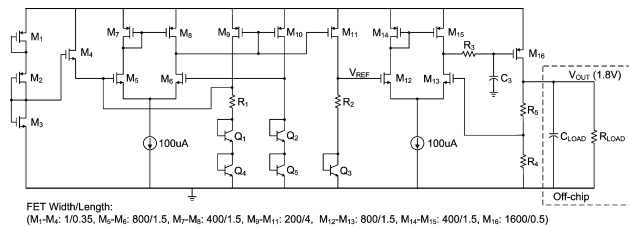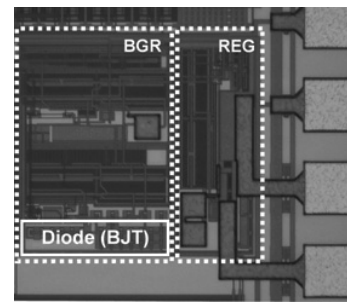upply voltage to various RF building blocks in the transmitter IC. The input voltage of the LDO is required to be in the range of 3.3–5 V, which is provided from the system application board. In order to support the rather wide input voltage range, the regulator is designed by using 3.3 V MOSFETs with nominal threshold voltage in the $0.18\,\mu$m 1-poly 6-metal RF CMOS process. Figure 3 shows the designed circuit schematic of the LDO and BGR, in which the designed values of the gate widths and lengths of all FETs are shown together. To tolerate up to 5 V of the input voltage, the pass-FET M_{16} has a gate length of $0.5\,\mu$m, and the other FETs have even greater length.

The regulator employs the stacked diodes of Q_1, Q_2, Q_4, and Q_5 to reduce the output noise. The area ratios of the stacked diodes Q_1/Q_2 and Q_4/Q_5 are 7 and 15, thus the overall area ratio is 105. The area saving factor is 4.77 according to (6). With such a high area ratio of 105, R_2/R_1 can be set to a small value of 2.1 as desired for low output noise. The designed values of R_1 and R_2 are $375\,\Omega$ and $800\,\Omega$, respectively. Meanwhile, R_3 and C_3 are used primarily as a frequency compensation element and also as a low pass filter for further suppression of the noise transferred through the pass transistor M_{16}. Three FETs M_{13}–M_{15} constitute a start-up circuit. The total current consumption of the LDO is 1.2 mA, of which the BGR consumes most of the current of 1.0 mA.

The circuit is fabricated in TSMC $0.18\,\mu$m RF CMOS technology. Figure 4 shows the chip micrograph. The total silicon area is $280 \times 250\,\mu$m^2. The diode section occupies $5{,}100\,\mu$m^2, which would be as high as $24{,}330\,\mu$m^2 if not with the stacked diode structure.

The LDO is packaged in 48-pin leadless plastic chip carrier (LPCC) and tested on an evaluation board. The off-chip capacitance C_{LOAD} at the output is set as low as 100 nF without having any oscillation problem. Figure 5 shows the
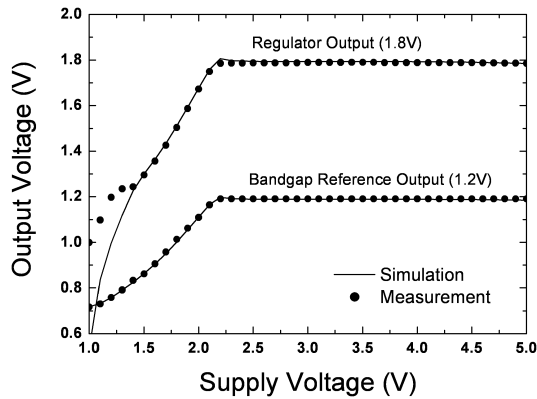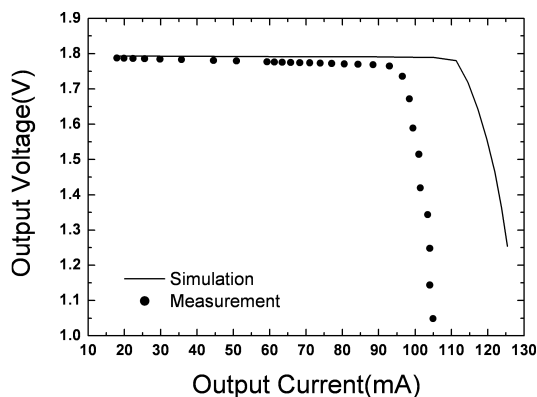
Fig. 5 Measured line regulation.

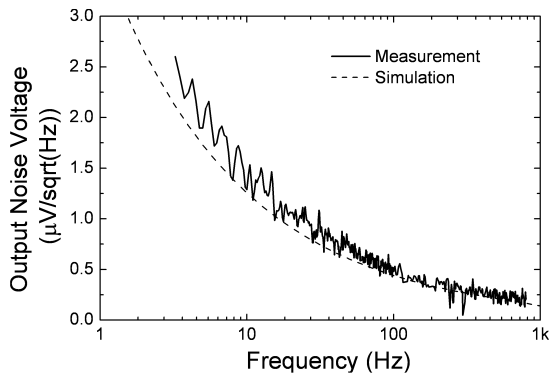**Fig. 6** Measured load regulation.

Fig. 7 Measured output spectral noise.

line regulation performance. The measured line regulation is 0.04%/V. The measurement and simulation results show good agreement. The measured dropout voltage is 0.3 V. Figure 6 shows the measure load regulation. It is 0.46% for the output current of 50 mA, whereas it increases up to 1% for the higher output current of 90 mA. The measured load regulation is worse than the simulated result. It is attributed to an unexpectedly high parasitic resistance involved at the output terminal path. The output spectral noise is measured and shown in Fig. 7. The output noise is 479 and 186 nV/sqrt(Hz) at 100 Hz and 1 kHz, respectively. It should

Table 1 Performance summary and comparison.

	This work	[3]	[4]
Technology	0.18 μm CMOS	0.35 μm CMOS	0.6 μm CMOS
Input Supply Voltage	2.2 ~ 5 V	1.5 ~ 4.5 V	1.5 ~ 4.5 V
Output Voltage	1.8 V	1.2 V	1.3 V
Line Regulation	0.04 %/V	0.057 %/V	0.5 %
Load Regulation	0.46 % @ ΔI_{LOAD} = 50mA	0.133 %	0.5 %
Output Noise Density (nV/√Hz) @ offset frequency	479 @ 100Hz 186 @1kHz	2701 @ 20 kHz	1800 @ 100 Hz 380 @ 100 kHz
Peak Output Current	90 mA (1% variation)	120 mA	100 mA
Current Consumption	BGR = 1.1 mA REG = 110 μA	NA	38 μA (Regulator only)
Active Area	282 x 250 mm²	360 x 345 mm²	568 x 541 mm²

be pointed out that the output noise of this work is remarkably lower than the typical values reported in the literature. The overall performance of the fabricated LDO is summarized and compared with other similar LDOs in Table 1.

4. Conclusion

A low output noise LDO employing an area-efficient bandgap reference by using the stacked diode structure is presented. For the bandgap reference, a high effective area ratio of 105 has been realized with an area saving factor of 4.77. Implemented in 0.18 μm CMOS, the LDO achieves the remarkably low output noise of 186 nV/sqrt(Hz) at 1 kHz.

Acknowledgments

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