Analog CMOS Integrated Circuit Design
Design Project: Opamp Design

The objective of this project is to design and simulate a differential input single-ended output CMOS operational amplifier (opamp) that meets the specifications given in Table 1. The opamp is intended for use in a unity-gain feedback circuit shown in Fig. 1.

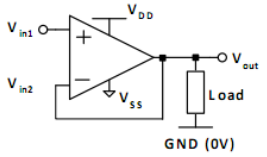

Figure 1. Opamp in unity-gain feedback (i.e., unity buffer)

Process	0.35 μm CMOS
V_{DD}	1.5 V
V_{SS}	–1.5 V
Load	10 pF
A_{DM0} (low-frequency open-loop small-signal gain)	≥ 70 dB
A_{CM0} (low-frequency open-loop small-signal common-mode gain)	≤ –10 dB
Phase margin	≥ 60°
Unity gain frequency	≥ 10 MHz
Slew rate (both positive and negative)	≥ 10 V/μs
Nominal input common-mode voltage	0 V
Input common-mode range	–0.2 to 0.2 V
Output voltage swing (peak to peak)	≥ 1.2 V
Power	≤ 500 μW

Table 1. Design Specifications

For this design only NMOS, PMOS transistors and capacitors can be used and you need to use the 0.35μm CMOS technology whose model file is:
/CMC/kits/cmosp35/models/hspice/mm0355v.l
In your op-amp design, you can use one (and only one) ideal dc current source as a bias generator and generate all the other required bias currents from this current source. Note that the overall power consumption of your circuit includes the power of this ideal current source. Other than V_{DD} and V_{SS}, you cannot use any other ideal voltage source. If you need a bias voltage, you have to design a circuit to create that voltage.

The unity gain buffer of Fig. 1 is to be used for sinusoidal signals with frequencies less than 5 MHz. In your project report, include the output transient response of your opamp, configured as Fig. 1, for a sinusoidal input with amplitude of 0.6 V (1.2 V peak to peak) and frequency of 5 MHz. The output signal should closely resemble to input without any visible distortion
Furthermore, please include the transient output responses for four different input steps with amplitudes of 0.1V, 1V, -0.1V, and -1V. Measure and report the initial rising/falling slopes of the output and also the 1% settling times (this is the time required for the output to reach within 1% of its final value). To report your project and the SPICE code of your design, please follow these steps:

1. Put your SPICE file and any other relevant file such as your project report in the document .
2. You need to handin at least your spice code and a document which includes your name, student number, a table summarizing the performance results of your opamp, summary of your hand calculations and a brief description of your design approach, required plots including the bode plot of open-loop transfer function on which achieved phase margin and low frequency gain are annotated, bode plot of closed-loop system on which the 3dB frequency of the system is indicated, and any comments and conclusions. Please also include the schematic of your design with transistor sizes and bias currents indicated on the schematic beside each transistor (component values should be indicated beside each component).